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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,081	09/26/2003	Juju Joyce	015114-066300US	7487

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,081	JOYCE ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-12 and 14-22* is/are rejected.

7)☒ Claim(s) *2 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This office action responsive to communication filed 06/14/2004. Claims 1-22 are presented for examination.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-4, 7-8, 12, 14-15 and 19 are rejected under 35 U.S.C. § 102(b) as being anticipated by Mahoney et al. (USPN: 5,694,056); hereinafter Mahoney.

As per claims 1 and 12; Mahoney discloses the invention as claimed including a system and method for transferring data in parallel from an external memory device to an integrated circuit (e.g. see abstract; column 1, lines 65 et seq.), the method comprises transferring a start address from the integrated

circuit to the external memory device, providing a clock signal generated by the integrated circuit to the external memory device, sequentially generating read addresses in response to the clock signal beginning with the start address using an address counter in the external memory device is equivalently taught as configuration data are transferred into an integrated circuit (IC) using a serial data stream and transfer mechanism wherein the configuration data is transferred into the IC in sequential frames of specified size for a given IC. The first bit of the configuration data contains a frame full indicator. The configuration data is transferred into a shift register circuit and the last bit position(s) of the shift register circuit, in addition to being stored in the shift register circuit, are shifted along a special frame full pipeline to a control unit (e.g. see column 2, lines 7-17); reading data stored in the external memory device at the read addresses; and transferring data in parallel from the external memory device to the integrated circuit is taught as a parallel write command is asserted that causes the data of the shift register circuit to be parallel transferred to a receiving column of memory (e.g. see column 2, lines 17-19).

As per claims 3-4 and 14-15; Mahoney discloses that the external memory operate in a sequential read mode when the clock

signal toggles or when the sequential read command is received (e.g. see figures 2 and 3; column 7, lines 5 et seq.);

As per claims 7 and 18; Mahoney discloses the integrated circuit is a field programmable gate array and the data is configuration data (e.g. see column 1, lines 8-10; column 2, lines 9 et seq.);

As per claims 8 and 19; Mahoney discloses the integrated circuit is a programmable integrated circuit that is part of a digital system that includes a processor (control unit 180) (e.g. see column 1, lines 12 et seq.; figure 1);

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5-6, 9-11, 16-17 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahoney et al. (USPN: 5,694,056); hereinafter Mahoney.

As per claims 5-6 and 16-17; Mahoney discloses the invention as claimed, detailed above with respect to claims 1 and 12. Mahoney only illustrates one IC chip in his invention, Manhoney does not particularly teach multiple IC chips are employed and being daisy-chained or cascaded to receive the transferred data wherein one of the IC is a master device. However; it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the system of Mahoney in multiple ICs environment wherein IC are being cascaded for receiving transferred data, since cascading of integrated circuit is commonly known in the memory storage art for improving data storage; in addition, by implementing the system of Mahoney in a daisy-chaining environment, it would reduce total address lines requires for accessing information in the individual memory IC/module, free up the system address-lines for other operations which results to increasing overall system throughput and performance, therefore being advantageous.

As per claims 9-10 and 20-21; the difference between Mahoney and the claims is the claims recites the data is transferred in parallel to the integrated circuit along 8 or 16 parallel signal lines. However, the specific size of the lines using for transferring data to the integrated circuit does not have a disclosed purpose nor are disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been obvious

matter to one skilled in the art to utilize 8 or 16 signal lines as in the system of Mahoney in order to transfer data in parallel or bulk to increase data transfer rate or system throughput.

As per claims 11 and 22, Mahoney discloses configuration data being transferred from the external memory to the IC circuit. Mahoney does not particularly show the type of external memory. Noting that, the specific type of memory for storing configuration data to transfer to the Integrated circuit also does not have a disclosed purpose nor are disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the external memory as FLASH memory type as being claimed for storing the configuration data, since FLASH or non-volatile memory is known for its versatile in that it eliminates the need for special battery backup circuits to preserve data store therein, therefore being advantageous.

Allowable subject matter

7. Claims 2 and 13 are objected to as being dependent upon a rejected based claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-41287. The examiner can normally be reached from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/August 18, 2006

Tuan V. Thai
PRIMARY EXAMINER
Group 2100